OTQ-100G-PSM4

100G PSM4 QSFP28 Transceiver

DESCRIPTION

The OTQ-100G-PSM4 100G QSFP28 PSM4 module assembly is a monolithic electronic and photonic module assembly containing four 1310nm optical lanes, each operating at data rates up to 25Gb/s. The optical interface of the module is a 12fiber MPO receptacle compliant to 100G PSM4 MSA. It provides an excellent solution for 100G applications where cost effective high port density is needed. It also provides backward compatibility in supporting 40G applications. The transceiver is compliant to QSFP28 MSA, PSM4 MSA and applicable portions of IEEE802.3bm.

FEATURES

- 1310nm DFB transmitter and PIN receiver
- Support multi rate 4x25Gb/s, 4x10Gbps and 4x4.25Gbps operation
- MPO-12 APC optical connector
- Compliant to 100G PSM4 MSA specifications
- Transmission distance up to 2km on SMF
- 3.3V power supply
- Low power consumption <3.5W (With CDR)
- Operating case temperature: 0~+70°C
- RoHS 6/6 compliant
- Hot-Pluggable

APPLICATION

- 100 Gigabit Ethernet
- Proprietary Cluster Interconnect
- Ethernet Local Area Network (LAN)

ABSOLUTE MAXIMUM RATINGS (TC=25°C, UNLESS OTHERWISE NOTED)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	TS	-40	-	+85	ºC	
Maximum Supply Voltage	Vcc	-0.3	-	3.6	V	
Operating Relative Humidity	RH	15	-	+85	%	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Data Rate	DR		103.1		Gb/s	
Operating Case Temperature	Top	0		70	ºC	
Bit Error Rate	BER			1E-12		
Fiber Length on SMF per G.652	L			2000	m	
Loss budget over SMF per G.652				3.6	dB	1
Supply Voltage	Vcc	3.135		3.465	V	
Module Total Power	P			3.5	W	normal mode
	P_W	-		1.5	W	Low power mode

Notes:

1. The channel insertion loss budget may include up to 1dB MPI loss penalty with worst case transmitter and worst case connector MPI.

QSFP28 Connector Pad Layout

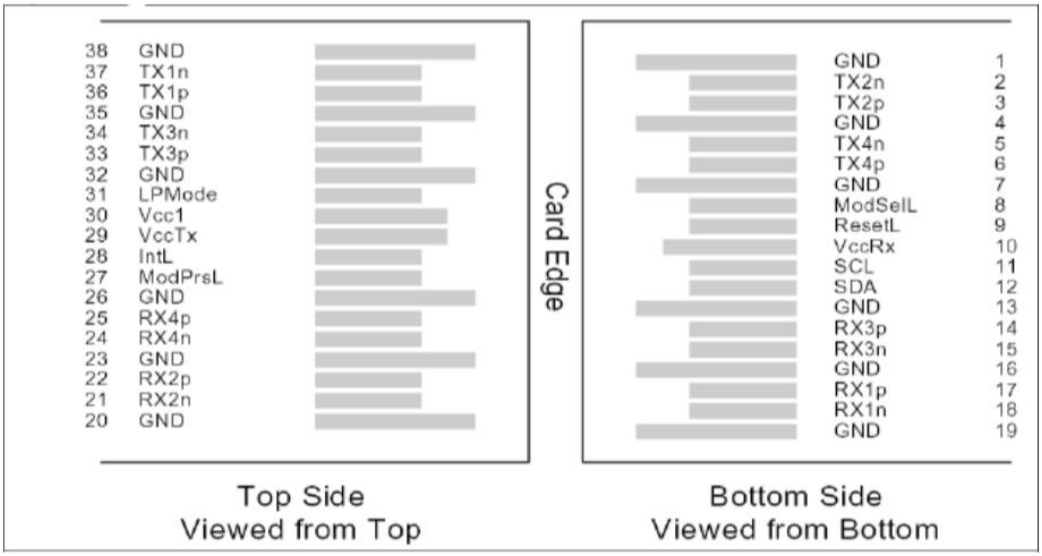


Figure 1 – QSFP28-Compliant 38-Pin Connector

PIN DESCRIPTIONS

Pin	Logic	Symbol	Name/Description
1	GND	GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4	GND	GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7	GND	GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10	VCC	Vcc_Rx	+3.3 V Power supply receiver
11	LVCMOS-I/O	SCL	2-wire serial interface clock
12	LVCMOS-I/O	SDA	2-wire serial interface data
13	GND	GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16	GND	GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19	GND	GND	Ground
20	GND	GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23	GND	GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26	GND	GND	Ground
27	LVTTL-O	ModPrsL	Module Present, grounded inside the module
28	LVTTL-O	IntL	Interrupt
29	VCC	VCC Tx	+3.3 V Power supply transmitter
30	VCC	VCC1	+3.3 V Power Supply
31	LVTTL-I	LPMode	Low Power Mode, active high
32	GND	GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input

Pin	Logic	Symbol	Name/Description
35	GND	GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38	GND	GND	Ground

ELECTRICAL SPECIFICATION

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Differential input impedance	Z_d	-	100	-	Ω	
Differential input voltage	-	100	-	1600	mV	
Differential termination mismatch	-	-	10	-	%	
Differential Input Return Loss@0.01–8 GHz	SDD11	9.5-0.37f	-	-	dB	1
Differential Input Return Loss@8 – 19 GHz		4.75-7.4log10(f/14)	-	-	dB	1
Differential to Common Mode Output Return Loss@0.01-12.89GHz	SCD11	22-20(f/25. 78)	-	-	dB	1
Differential to Common Mode Output Return Loss@12.89 – 19 GHz		15 - 6(f/25.7 8)		-	dB	1
BER with stressed input signal	-	-	-	$1x10^{-15}$		2
DC common mode voltage	-	-350	-	2850	mV	
Receiver						
Differential Output impedance	Z_d	-	100	-	Ω	
Differential Output Voltage	-	400	-	1200	mV	3
DC common mode voltage	-	-350		2850	mV	
AC common-mode output voltage	-	-	-	17.5	mV	
Vertical eye closure	VEC	-	-	5.5	dB	
Eye width	-	0.57	-	-	UI	
Eye height, differential	-	228	-	-	mV	
Rx Output Data Total Jitter	-	-	-	0.43	UI	
Transition Time (min, 20% to 80%)	t_{RH},t_{FH}	12	-	-	P_S	
Differential Output Return Loss@ 0.01–8 GHz	SDD22	9.5-0.37f	-	-	dB	1
Differential Output Return Loss@ 8 – 19 GHz		4.75-7.4log10(f/14)	-	-	dB	1
Common Mode to Differential Output Return loss@ 0.01 -12.89 GHz	SDC22	22-20(f/25. 78)	-	-	dB	1
Common Mode to Differential Output Return loss@12.89 – 25.78 GHz		15 - 6(f/25.7 8)	-	-	dB	1

Notes:
[1] f is frequency in GHz
[2] per IEEE802.3bm Annex 83E.3.4.1
[3] Differential output voltage amplitude is adjustable through I2C bus. Default value of the differential output voltage amplitude per lane is 400 – 800 mV

LOW SPEED ELECTRICAL INTERFACE

Parameter	Symbol	Min	Typical	Max	Units	Notes
SCL and SDA	V_{OL}	0	-	0.4	V	1
	V_{OH}	Vcc-0.5	-	Vcc+0.3	V	
	V_{IL}	-0.3	-	Vcc*0.3	V	
	V_{IH}	Vcc*0.7	-	Vcc+0.5	V	
LPMode, Reset and ModSelL	V_{IL}	-0.3	-	0.8	V	
	V_{IH}	2	-	Vcc+0.3	V	
ModPrsL and IntL	V_{OL}	0	-	0.4	V	
	V_{OH}	Vcc-0.5	-	Vcc+0.3	V	

Notes:
[1] IOL (max) =3.0mA; Capacitance for SCL and SDA I/O pin less than 14pF; Total bus capacitive load for SCL and SDA less than 100pF with maximum 3.0kΩ pull-up resistor (less than 200pF with maximum 1.6kΩ pull-up resistor)

OPTICAL SPECIFICATION

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Signaling Speed (±100ppm, per Lane)	B	-	25.78125	-	Gb/s	
Center Wavelength	λ	1295	1310	1325	nm	
Total average launch power(All Lane)	-	-	-	+8	dBm	
Average launch power, each lane	Pavg	-9.4	-	2	dBm	1
Difference in launch power between any two lanes (OMA)	-	-	-	5	dB	
Optical Modulation Amplitude (per Lane)	P_{OMA}	-4	-	2.2	dBm	
Tx_OMA-TDP	-	-5			dBm	
Extinction Ratio	ER	3.5	-	-	dB	
Transmitter and dispersion penalty (TDP), each lane	TDP	-	-	2.9	dB	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Average Launch Power of OFF Transmitter	P_{off}	-	-	-30	dBm	
RIN OMA	-	-	-	-128	dB/HZ	
Transmitter reflectance	-	-	-	-12	dB	
Optical return loss tolerance	ORL	-	-	20	dB	
Optical Output Eye	Compliant with PSM4 MSA {0.31, 0.4, 0.45, 0.34, 0.38, 0.4}					

Parameter		Symbol	Min	Typical	Max	Units	Notes
Receiver							
Lane Wavelengths		λ	1295	1310	1325	nm	
Average Receive Power (per Lane)		-	-12.66	-	2	dBm	2
Rx OMA (per lane)		-	-	-	2.2	dBm	
Receiver Sensitivity (OMA), each lane	4.25Gbps,1E-12	R_{sens}	-	-	-8.6	dBm	3
	10Gbps,1E-12				-8.6	dBm	4
	25.78Gbps,5E-5				-11.35	dBm	5
	25.78Gbps,1E-12		-	-	-8.6	dBm	6
Damage Threshold		-	3	-	-	dBm	
Stressed Sensitivity in OMA (per lane)		-	-	-	-8.79	dBm	5
Conditions of stressed receiver sensitivity test:							
Vertical eye closure penalty, each lane		VECP	1.9	-	-	dB	
Stressed eye J2 Jitter, each lane		-	0.27	-	-	UI	
Stressed eye J4 Jitter, each lane		-	0.39	-	-	UI	
Stressed eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.24,0.5,0.5,0.24,0.24,0.4}					
Receiver Reflectance		-	-	-	-26	dB	
LOS Hysteresis		-	0.5	-	6	dB	
LOS Thresholds	Increasing Light Input	P_{los+}	-	-	-12	dBm	7
	Decreasing Light Input	P_{los-}	-30	-	-	dBm	

Notes:
[1] Average launch power is informative and not the principal indicator of signal strength. A transmitter with launch power below the min value cannot be compliant; however, a value above it does not ensure compliance.
[2] Average receive power is informative and not the principal indicator of signal strength. A received power below the min value cannot be compliant; however, a value above it does not ensure compliance.
[3] Receive sensitivity measured at BER less than 1E-12, with a 2^31-1 PRBS @4.25Gbps,
[4] Receive sensitivity measured at BER less than 1E-12, with a 2^31-1 PRBS @10Gbps,
[5] Receive sensitivity measured at BER less than 5E-5, with a 2^31-1 PRBS @25.78Gbps,
[6] Receive sensitivity measured at BER less than 1E-12, with a 2^31-1 PRBS @25.78Gbps,
[7] In average power.

DIGITAL DIAGNOSTIC FUNCTIONS

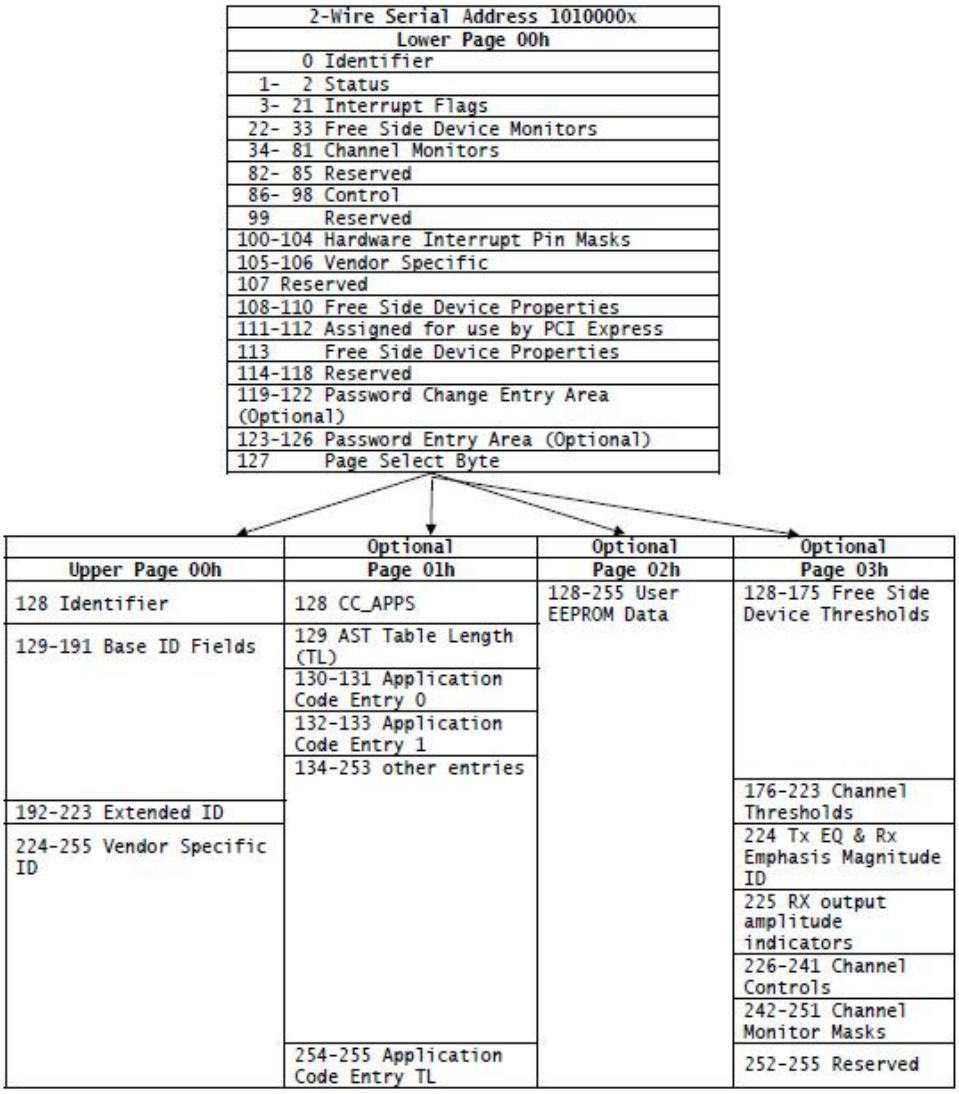


Figure 2 – Two-Wire Interface Fields

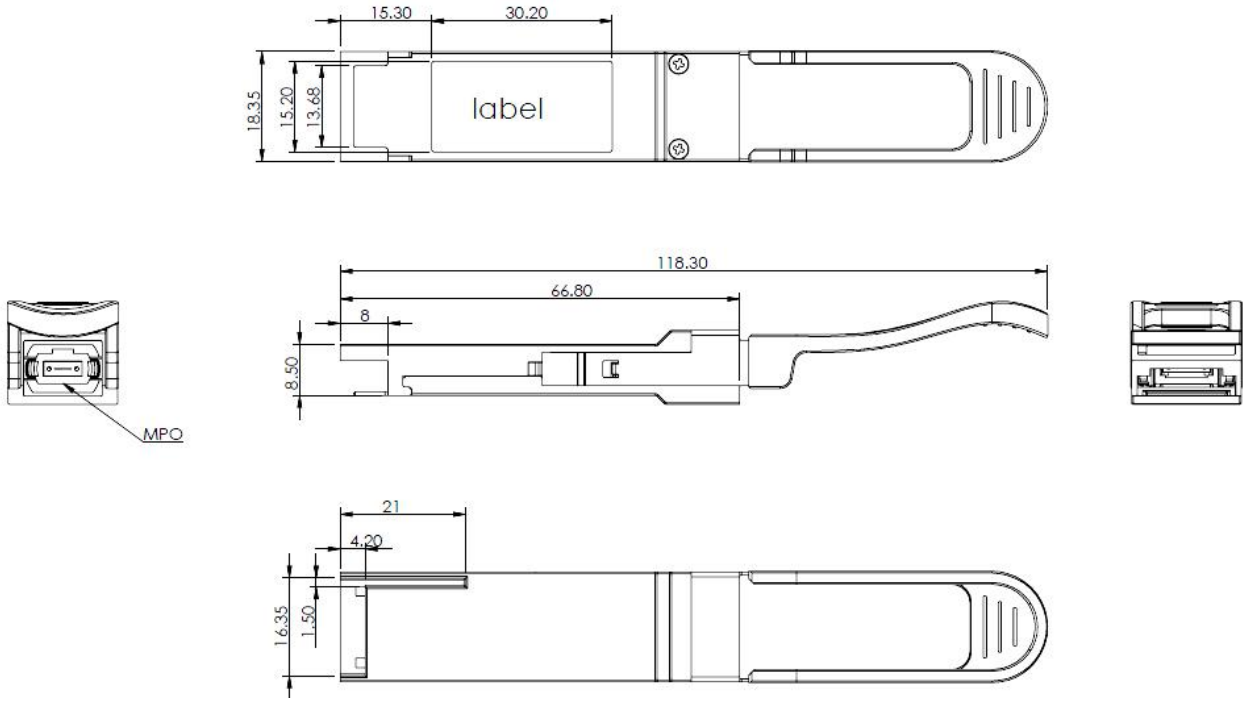
The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through a 2-wire serial interface. The 2-wire serial interface shall consist of a master and slave. The fixed side shall be the master and the free side shall be the slave. Control and data are transferred serially. The master shall initiate all data transfers. Data can be transferred from the master to the slave and from the slave to the master. The 2-wire interface shall consist of clock (SCL) and data (SDA) signals. The master utilizes SCL to clock data and control information on the 2-wire bus. The master and slave shall latch the state of SDA on the positive transitioning edge of SCL. The SDA signal is bi-directional. During data transfer, the SDA signal shall transition when SCL is low. A transition on the SDA signal while SCL is high shall indicate a stop or start condition.
For more information, please see the QSFP28 MSA documentation.

DIGITAL DIAGNOSTIC SPECIFICATIONS

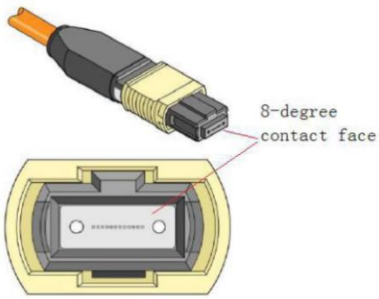
Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Case Temperature	DMI_Temp	-3		+3	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-3%		+3%	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-3		+3	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%		+10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-3		+3	dB	Per channel

MECHANICAL SPECIFICATIONS

Unit: mm



To minimize MPO connection induced reflections, an MPO receptacle with 8-degree angled end-face is utilized for this product. A female MPO connector with 8-degree end-face should be used with this product as illustrated in below.



ORDERING INFORMATION

OTQ-100G-PSM4

ESD SAFETY CAUTIONS

This transceiver is specified as ESD threshold 1KV for high speed data pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.